Set   Items   Description
S1   6   AU='COLABELLA':AU='COLABELLA C E'

File 347:JAPIO Oct 1976-2002/Dec(Updated 030402)
          (c) 2003 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2003/Apr W02
          (c) 2003 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20030417,UT=20030410
          (c) 2003 WIPO/Univentio
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200325
          (c) 2003 Thomson Derwent

                              EKD   April 22, 2003

1/5/1   (Item 1 from file: 348)

00990993
Process for realizing cross-point memory devices with cells having a source channel which is self-aligned to the bit line and to the field oxide
Herstellungsprozess von Kreuzpunktspeicherbauelementen mit Zellen, die einen zur Bitleitung und zum Feldoxyd selbstjustierten Source-Kanal aufweisen
Procede de fabrication de dispositifs de memoire a points de croisement avec des cellules ayant un canal source qui est auto aligne avec la ligne de bit et l'ox
PATENT ASSIGNEE:
  STMicroelectronics S.r.l., (1014060), Via C. Olivetti, 2, 20041 Agrate
    Brianza (Milano), (IT), (applicant designated states:
    AT;BE;CH;DE;DK;ES;FI;FR;GB;GR;IE;IT;LI;LU;MC;NL;PT;SE)
INVENTOR:
  Colabella , Elio, Via Paracelso, 10, 20100 Milano (MI), (IT
LEGAL REPRESENTATIVE:
  Botti, Mario (87642), Botti & Ferrari S.r.l. Via Locatelli, 5, 20124
    Milano, (IT)
PATENT (CC, No, Kind, Date): EP 896369 A1   990210 (Basic)
APPLICATION (CC, No, Date):   EP 97830418 970808;
PRIORITY (CC, No, Date): EP 97830418 970808
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: H01L-021/8247;

ABSTRACT EP 896369 A1
    The invention relates to a process of manufacturing cross-point matrix
  memory devices which have floating gate memory cells having the source
  channel self-aligned to the bit line and the field oxide.
    The process comprises the steps of:
    growing a thin layer (3) of tunnel oxide on the matrix region;
    depositing a stack structure comprising a first conductive layer (4),
  an intermediate dielectric layer (5), and a second conductive layer (6);
    photolithographing with a Poly1 mask to define a plurality of parallel
  floating gate regions (13) in said stack structure;
    self-aligned etching of said stack structure (4,5,6), above the active
  areas, to define continuous bit lines;
    implanting, to confer predetermined conductivity on the active areas
  (10). Advantageously, the self-aligned cascade etching step for removing
  parallel strips from multiple layers, down to the active areas of the
  substrate (1), is discontinued before the field oxide (2) is removed, and
  the implantation step is carried out in the presence of field oxide (2)
  over the source active areas (10).
ABSTRACT WORD COUNT: 172

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 990210 A1 Published application (A1with Search Report
                              ;A2without Search Report)
 Change: 990428 A1 Representative (change)
 Examination: 990818 A1 Date of request for examination: 19990622
LANGUAGE (Publication,Procedural,Application): English; English; Italian
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9906	247
SPEC A	(English)	9906	2455
Total word count - document A			2702
Total word count - document B			0
Total word count - documents A + B			2702

1/5/2   (Item 2 from file: 348)

00933813
Self-aligned etching process to realize word lines of semiconductor integrated memory devices
Selbstjustiertes Atzverfahren zur verwirklichung der Wortleitungen integrierter Halbleiterspeicherbauelemente
Procede de gravure auto-alignee pour la realisation des lignes de mot des dispositifs de memoire integree semi-conductrice

PATENT ASSIGNEE:
  STMicroelectronics S.r.l., (1014060), Via C. Olivetti, 2, 20041 Agrate Brianza (Milano), (IT), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
  Camerlenghi, Emilio, Via Zendrini, 2, 24100 Bergamo, (IT)
   Colabella , Elio, Via Paracelso, 10, 20100 Milano, (IT)
  Pividori, Luca, Via G. Cravero, 14, 10100 Torino, (IT)
  Rebora, Adriana, SGS-Thomson Microelectronics Srl, Via C. Olivetti, 2, 20041 Agrate Brianza (Milano), (IT
LEGAL REPRESENTATIVE:
  Botti, Mario (87642), Botti & Ferrari S.r.l. Via Locatelli, 5, 20124 Milano, (IT)

ABSTRACT EP 851485 A1
    Self-aligned etching process for providing a plurality of mutually parallel word lines in a first conducting layer (11,12) deposited over a planarized architecture (9) obtained starting from a semiconductor substrate (1) on which is provided a plurality of active elements extending along separate parallel lines e.g. memory cell bit lines (13) and comprising gate regions made up of a first conducting layer (4), an intermediate dielectric layer (5) and a second conducting layer (6) with said regions being insulated from each other by insulation regions (7,8) to form said architecture (9) with said word lines being defined photolithographically by protective strips implemented by means of:
    - a vertical profile etching for complete removal from the unprotected areas of the first conducting layer (11,12), of the second conducting layer (6) and of the intermediate dielectric layer (5) respectively, and
    - a following isotropic etching of the first conducting layer (4).
ABSTRACT WORD COUNT: 150

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 980701 A1 Published application (A1with Search Report ;A2without Search Report)
*Assignee: 980826 A1 Applicant (name, address) (change)
 Examination: 990303 A1 Date of filing of request for examination: 981221
 Change: 990317 A1 Designated Contracting States (change)
 Change: 990428 A1 Representative (change)
LANGUAGE (Publication,Procedural,Application): English; English; Italian
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9827	306
SPEC A	(English)	9827	2278
Total word count - document A			2584
Total word count - document B			0
Total word count - documents A + B			2584

00933812

Self-aligned etching process to realize word lines of semiconductor
    integrated memory devices
Selbstjustiertes Atzverfahren zur Verwirklichung der Wortleitungen
    integrierter Halbleiterspeicherbauelemente
Procede de gravure auto-alignee pour la realisation des lignes de mot des
    dispositifs de memoire integree semi-conductrice
PATENT ASSIGNEE:
  STMicroelectronics S.r.l., (1014060), Via C. Olivetti, 2, 20041 Agrate
    Brianza (Milano), (IT), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
  Colabella , Elio, Via Paracelso, 10, 20100 Milano, (IT)
  Pividori, Luca, Via G. Cravero, 14, 10100 Torino, (IT)
  Rebora, Adriana, SGS-Thomson Microelectronics Srl, Via C. Olivetti, 2,
    20041 Agrate Brianza (Milano), (IT
LEGAL REPRESENTATIVE:
  Botti, Mario (87642), Botti & Ferrari S.r.l. Via Locatelli, 5, 20124
    Milano, (IT)
PATENT (CC, No, Kind, Date): EP 851484 A1 980701 (Basic)
APPLICATION (CC, No, Date):   EP 96830648 961224;
PRIORITY (CC, No, Date): EP 96830648 961224
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: H01L-021/8247

ABSTRACT EP 851484 A1
    The process proposed allows provision of a matrix topography for
    electronic memory devices using self-alignment etchings capable of
    removing those spurious electrical contacts between adjacent memory
    cells.
    The self-aligned etching process proposed for providing a plurality of
    mutually parallel word lines in a first conducting layer (11,12)
    deposited over a planarized architecture (9) obtained starting from a
    semiconductor substrate (1) on which is provided a plurality of active
    elements extending along separate parallel lines e.g. memory cell bit
    lines (13) and comprising gate regions formed by a first conducting layer
    (4), a dielectric interpoly layer (5) and a second conducting layer (6)
    with said regions being insulated from each other by dielectric
    insulation films(7,8) to form said architecture (9) with said word lines
    being defined photolithographically by protective strips is implemented
    by means of:
    - a vertical profile etching for complete removal from the unprotected
    areas respectively of the first conducting layer (11,12), of the second
    conducting layer (6) of the gate region,
    - a successive etching of the dielectric interpoly layer (5) accompanied
    by a considerable erosion of the dielectric film (8) of the insulation
    region so as to totally uncover the first conducting layer (4), and
    - a concluding etching of the first conducting layer (4).
ABSTRACT WORD COUNT: 209

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 980701 A1 Published application (A1with Search Report
                              ;A2without Search Report)
 *Assignee: 980826 A1 Applicant (name, address) (change)
 Examination: 990303 A1 Date of filing of request for examination:
                              981221
 Change: 990317 A1 Designated Contracting States (change)
 Change: 990428 A1 Representative (change)
LANGUAGE (Publication,Procedural,Application): English; English; Italian
FULLTEXT AVAILABILITY:
Available Text Language   Update   Word Count
      CLAIMS A (English) 9827   337
      SPEC A   (English) 9827   2625
Total word count - document A   2962
Total word count - document B   0
Total word count - documents A + B   .2962

00933809
**Process for deposing a stratified dielectric for enhancing the planarity of
    semiconductor electronic devices**
**Verfahren   zur   Abscheidung   eines   geschichteten   Dielektrikums   zur
    Verbesserung der Planaritat von elektronischen Halbleiterschaltungen**
**Procede de depot d'un dielectrique stratifie pour augmenter la planeite de
    dispositifs electroniques semi-conducteurs**
PATENT ASSIGNEE:
  STMicroelectronics S.r.l., (1014060), Via C. Olivetti, 2, 20041 Agrate
    Brianza (Milano), (IT), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
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   Colabella , Elio, Via Paracelso, 10, 20100 Milano, (IT)
  Bacchetta, Maurizio, Via Galvani, 2, 20093 Cologno Monzese (Milano), (IT)
  Pividori, Luca, Via G. Cravero, 14, 10100 Torino, (IT
LEGAL REPRESENTATIVE:
  Botti, Mario (87642), Botti & Ferrari S.r.l. Via Locatelli, 5, 20124
    Milano, (IT)
PATENT (CC, No, Kind, Date): EP 851470 A1 980701 (Basic)
APPLICATION (CC, No, Date):   EP 96830645 961224;
PRIORITY (CC, No, Date): EP 96830645 961224
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: H01L-021/3105

ABSTRACT EP 851470 A1
    A plurality of bit lines (6) are isolated from one another by a layered
    dielectric structure to provide a planar architecture onto which an
    optional conductive layer may be deposited.
    The dielectric structure deposited with the method proposed in the
    instant Patent Application uses a highly planarizing dielectric layer
    (18) of the SOG type spun over a first insulating dielectric layer (17)
    and then solidified by means of a thermal polymerization process. The
    dielectric layers (17,18) are subjected to a etch-back treatment and to a
    subsequent thermal annealing treatment.
ABSTRACT WORD COUNT: 90

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Examination: 010919 A1 Date of dispatch of the first examination
                              report: 20010806
 Application: 980701 A1 Published application (A1with Search Report
                              ;A2without Search Report)
*Assignee: 980826 A1 Applicant (name, address) (change)
 Examination: 990303 A1 Date of filing of request for examination:
                              981221
 Change: 990317 A1 Designated Contracting States (change)
 Change: 990428 A1 Representative (change)
LANGUAGE (Publication,Procedural,Application): English; English; Italian
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9827	477
SPEC A	(English)	9827	2804
Total word count - document A			3281
Total word count - document B			0
Total word count - documents A + B			3281

00933808
Process for deposing a multiple dielectric structure for enhancing the

planarity of semiconductor electronic devices
Verfahren zur Abscheidung einer dielektrischen Vielfachstruktur zur
    Verbesserung der Planaritat von elektronischen Halbleitereinrichtungen
Procede pour deposer une structure multiple dielectrique pour augmenter la
    planarisation des dispositifs semi-conducteurs electroniques
PATENT ASSIGNEE:
  STMicroelectronics S.r.l., (1014060), Via C. Olivetti, 2, 20041 Agrate
    Brianza (Milano), (IT), (applicant designated states: DE;FR;GB;IT)
INVENTOR:
  Sonego, Patrizia, Via Marco Aurelio, 44, 20100 Milano, (IT)
   Colabella , Elio, Via Paracelso, 10, 20100 Milano, (IT)
  Bacchetta, Maurizio, Via Galvani, 2, 20093 Cologno Monzese (Milano), (IT)
  Pividori, Luca, Via G. Cravero, 14, 10100 Torino, (IT
LEGAL REPRESENTATIVE:
  Botti, Mario (87642), Botti & Ferrari S.r.l. Via Locatelli, 5, 20124
    Milano, (IT)
PATENT (CC, No, Kind, Date): EP 851479 A1 980701 (Basic)
APPLICATION (CC, No, Date): EP 96830644 961224;
PRIORITY (CC, No, Date): EP 96830644 961224
DESIGNATED STATES: DE; FR; GB; IT
INTERNATIONAL PATENT CLASS: H01L-021/768

ABSTRACT EP 851479 A1
    A method of depositing a dielectric ply structure to optimize the
planarity of electronic devices which include a plurality of active
elements having gate regions laid across the substrate as discrete
parallel lines, such as the bit lines of memory cells.
    The proposed solution in accordance with the principles of this
invention allows the plurality of bit lines to be isolated from one
another by a suitable dielectric ply structure to provide a planar
architecture onto which an optional conductive layer may be deposited.
    A plurality of word lines can be formed from the conductive layer by
conventional photolithographic and dry-wet etching processes.
    These lines intersect the plurality of bit lines to define a plurality
of EPROM cells organized into a matrix-like topography.
    The resulting planarization is adequate to avoid the typical
shortcomings of the prior art, such as the lack of electrical continuity
in the word lines or their excessively high electrical resistance from
slenderized portions in the conductive sections due to poor planarity of
the surfaces whereon the conductive layer is deposited.
ABSTRACT WORD COUNT: 175

LEGAL STATUS (Type, Pub Date, Kind, Text):
 Application: 980701 A1 Published application (A1with Search Report
                             ;A2without Search Report)
*Assignee: 980826 A1 Applicant (name, address) (change)
 Examination: 990303 A1 Date of filing of request for examination:
                             981221
 Change: 990317 A1 Designated Contracting States (change)
 Change: 990428 A1 Representative (change)
LANGUAGE (Publication,Procedural,Application): English; English; Italian
FULLTEXT AVAILABILITY:
Available Text Language   Update   Word Count
      CLAIMS A (English)   9827   741
      SPEC A   (English)   9827   3263
Total word count - document A   4004
Total word count - document B   0
Total word count - documents A + B   4004

 1/5/6   (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015195609   **Image available**
WPI Acc No: 2003-256139/200325

                        EKD   April 22, 2003

XRPX Acc No: N03-197046
**Account management method in financial service industry, involves
automatically providing reason for not closing account to customer, if
account is determined to be coded to close**
Patent Assignee: COLABELLA C E (COLA-I)
Inventor: **COLABELLA C E**
Number of Countries: 001   Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030018552	A1	20030123	US 2001911123	A	20010723	200325	B

Priority Applications (No Type Date): US 2001911123 A 20010723
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030018552	A1		10	G06F-017/60	

Abstract (Basic): US 20030018552 A
        NOVELTY - A status information associated with the identifier of
the account of user is retrieved. The closing of account is determined
from the retrieved status information. The reason for not closing the
account is automatically provided, if the account is determined to be
coded to close.
        DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the
following:
        (1) account management system; and
        (2) method for informing a user about status of the account.
        USE - For account management in financial service industry such as
credit card company.
        ADVANTAGE - Provides an automated system to handle calls from
customers and to reply status in response to call received from
customers. Thus, the cost in managing the customer service
representatives is reduced.
        DESCRIPTION OF DRAWING(S) - The figure shows the automated account
status system.
        Dwg.1/3
Title Terms: ACCOUNT; MANAGEMENT; METHOD; FINANCIAL; SERVICE; INDUSTRIAL;
  AUTOMATIC; REASON; CLOSE; ACCOUNT; CUSTOMER; ACCOUNT; DETERMINE; CODE;
  CLOSE
Derwent Class: T01
International Patent Class (Main): G06F-017/60
File Segment: EPI